

Gallium Arsenide

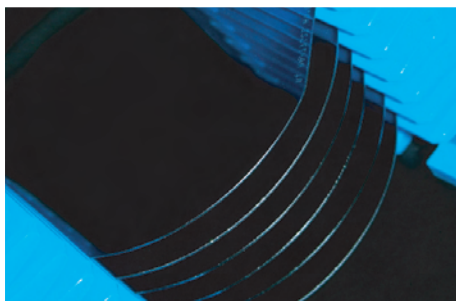
Epitaxy Ready Polished Wafers



Wafer Technology offers single crystal gallium arsenide grown at low pressure from high purity polycrystalline gallium arsenide in a vertical temperature gradient (VGF-Vertical Gradient Freeze). This method produces crystals with a much lower dislocation density than those produced by any other growth method

Mechanical Specifications

Gallium arsenide can be supplied as ingots or ingot sections or as-cut, etched or polished wafers. All gallium arsenide wafers are individually laser scribed with ingot and slice identity to ensure perfect traceability



Packaging

Polished Wafers

Fluoroware type tray, individually sealed in two outer bags in inert atmosphere. (Empak type boxes available on request)

As-cut Wafers

Empak type boxes (Glassine bag available on request)

'Process Trial' wafers

Fluoroware tray, individually sealed in one outer bag

If you do not see the specification you require, please ask for details

WAFER SPECIFICATIONS

	2" diameter slices	3" diameter slices	100mm diameter slices
Orientation	(100)±0.1°	(100)±0.1°	(100)±0.1°
	Misorientations up to 10° in direction =45° are routinely available. For other orientations and directions please ask.		
Diameter	50.5±0.5mm	76.2±0.4mm	100.0±0.5mm
Flat Option	EJ	EJ	EJ
	US/SEMI flat option is available.		
Flat orientation tolerance	±0.1°	±0.1°	±0.1°
	Wafers can also be supplied with either the major or minor flat prepared to an orientation tolerance of ± 0.02° to aid cleavage in laser manufacturing operations.		
Major flat length	16±2mm	22±2mm	32.5±2.5mm
Minor flat length	8±1mm	11±1mm	18±1mm
Thickness/μm	350±25μm or 500±25μm	625±25μm or 635±25μm	625±25μm or 635±25μm
Lasermark	Back surface parallel to major flat	Back surface parallel to major flat	Back surface parallel to major flat



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For all your III-V needs

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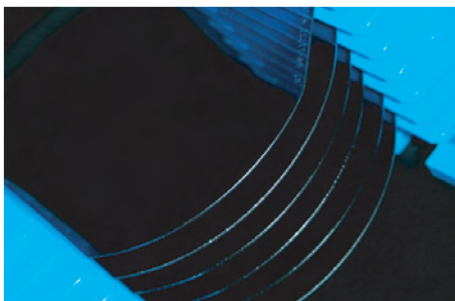


ELECTRONIC SPECIFICATIONS

Dopant	Type	Resistivity Ω cm	Carrier Concentration cm^{-3}	Mobility $\text{cm}^{-2}\text{V}^{-1}\text{s}^{-1}$	E.P.D. cm^{-2}
High Silicon	n-type	Not specified	$(1-5)\times 10^{18}$	Not specified	2" & 3" Grade 1 ≤ 100 Grade 2 ≤ 500 100mm ≤ 2000
Mid Silicon	n-type	Not specified	$(1-10)\times 10^{17}$	≥ 2000	2": ≤ 1500 3": ≤ 1500 100mm ≤ 3000
Low Silicon	n-type	Not specified	$\leq 3 \times 10^{16}$	≥ 4000	2": ≤ 3000 3": ≤ 5000
Tellurium	n-type	Not specified	$5 \times 10^{17} - 5 \times 10^{18}$	Not specified	2": ≤ 2000 3": ≤ 5000
Undoped	Semi-Insulating	$\geq 10^7$	Not Specified	≥ 5000	2": ≤ 2000 3": ≤ 5000 100mm ≤ 7000
Zinc	p-type	Not specified	$5 \times 10^{18} - 5 \times 10^{19}$	Not specified	2": ≤ 3000 3": ≤ 5000

Tighter electrical ranges are available on request

Wafer Technology also offers GaAs wafers produced by the High Pressure Liquid Encapsulated Czochralski (LEC) method. Single crystal ingots are produced using high purity gallium and arsenic as the starting material



ELECTRONIC SPECIFICATIONS

Dopant	Type	Resistivity Ω cm	Carrier Concentration cm^{-3}	Mobility $\text{cm}^{-2}\text{V}^{-1}\text{s}^{-1}$	E.P.D. cm^{-2}
Undoped	Semi-Insulating	$\geq 10^7$	Not Specified	≥ 5000	2": $\leq 5 \times 10^4$ 3": $\leq 1 \times 10^5$



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